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ORIGINAL PAPER

Formation of Al_2O_3–TiO_2 bilayer using atomic layer deposition and its application to dynamic random access memory

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Abstract To enhance film conformality together with electrical property suitable for dynamic random access memory (DRAM) capacitor dielectric, the effects of oxidant and post heat treatment were investigated on aluminum and titanium oxide (Al_2O_3–TiO_2) bilayer (ATO) thin film formed by atomic layer deposition method. For the conformal deposition of Al_2O_3 thin film, the O_3 oxidant required a higher deposition temperature, more than 450 °C, while H_2O or combined oxygen sources (H_2O+O_3) needed a wide range of deposition temperatures ranging from 250 to 450 °C. Conformal deposition of the TiO_2 thin film was achieved at around 325 °C regardless of the oxidants. The charge storage capacitance, measured from the ATO bilayer (4 nm Al_2O_3 and 2 nm TiO_2) deposited at 450 °C for Al_2O_3 and 325 °C for TiO_2 with O_3 oxidant on the phosphine-doped poly silicon trench, showed about 15% higher value than that of 5 nm Al_2O_3 single layer thin film without any increase of leakage current. To maintain the improved electrical property of the ATO bilayer for DRAM application, such as enhanced charge capacitance without increase of leakage current, upper electrode materials and post heat treatments after electrode formation must be selected carefully.

Dedicated to Professor Su-Il Pyun on the occasion of his 65th birthday.

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Keywords Atomic layer deposition · Al_2O_3 · TiO_2 · Thermal treatment · Leakage current density

Introduction

As the density of electronic devices have increased rapidly, the dielectric thin films for the gate oxide of metal-oxide-semiconductor field effect transistor, capacitor of dynamic random access memory (DRAM), and insulating layers in thin film electroluminescent devices require high dielectric constant (high-*k*) and low leakage current simultaneously [1–5]. SiO_2 thin film, grown by chemical vapor deposition (CVD) or thermal oxidation of silicon, was the typical dielectric with low leakage current. However, its low dielectric constant limited further applications. Such high-*k* materials as Y_2O_3, Ta_2O_5, Al_2O_3, HfO_2, and TiO_2 have received much attention due to their possibility for device being scaled down. However, most of the high-*k* materials showed poor insulating property due to their smaller barrier height with respect to the conduction level of Si [6].

Many researchers have tried to synthesize large charge storage capacitance with low leakage current by combining high leakage barrier materials and high-*k* materials, such as Al_2O_3–TiO_2, Al_2O_3–Ta_2O_5, Al_2O_3–HfO_2, and HfO_2–Ta_2O_5 [7–11]. These studies reported that the electrical properties of composite layers were greatly affected by film deposition condition and the following post thermal treatment. Atomic layer deposition (ALD) technique has been widely employed for composite dielectric thin film formation because of its self-limiting growth mechanism, uniform deposition, and accurate control of layer thickness even in the complex device structure [12, 13]. Much focus had been made not on the entire device, but on the intrinsic properties of the metal oxide thin film itself.

In this study, we studied not only the intrinsic properties of the Al_2O_3/TiO_2 bilayer (ATO) dielectric thin film, but also the post thermal effect of ATO considering device integration for DRAM. We firstly optimized single layer thin film formation of Al_2O_3 and TiO_2 using ALD on patterned structure with complex geometry, and then proceeded to ATO bilayer formation. Proper thickness combination of ATO improved its charge storage capacitance without increase of leakage current compared to that of Al_2O_3 single film. However, in applying ATO on DRAM capacitor full process, leakage current of ATO was closely related with fabrication conditions for DRAM device, such as the sort of upper electrodes and post thermal treatment.

Experimental details

ALD was achieved by using a showerhead type ALD reactor (Nano-ALD) supplied by IPS. The pressure during the deposition process was maintained to 133 Pa (1 Torr). Argon was used as a carrier and purging gas. The deposition conditions were summarized in Table 1. The thickness of Al_2O_3 and TiO_2 on Si (100) was measured by spectroscopic ellipsometry (ASET-F5x) provided by KLA-Tencor. The thickness of Al_2O_3 or TiO_2 on DRAM capacitor structure was also measured by Hitachi scanning electron microscopy (SEM) S-2600N. Deposition rate was defined as the thickness increase of the metal oxide per one ALD cycle (nm/cycle). ATO with various thicknesses was denoted as follows. For example, ATO with 4.0 nm thickness Al_2O_3 and 2.0 nm thickness TiO_2 was named as ATO-4.0-2.0. Lower electrode was composed of phosphine-doped poly Si (*p*-poly Si). The structure of lower electrode was on-cylinder structure (OCS), depicted in Fig. 1, to the maximize surface area of lower electrode. The height of the OCS was 1,500 nm and smallest hole width inside the OCS was 150 nm. ATO was deposited on the lower electrode. Subsequently, two layers of upper electrode were deposited on ATO. Barrier metal titanium nitride (TiN) was firstly deposited on ATO by CVD. Then tungsten (W) was subsequently formed by sputtering at ambient temperature or *p*-poly Si was deposited by CVD at 550 °C. In case of TiN/*p*-poly Si electrode, additional 650 °C annealing step in a nitrogen environment must be added to enhance the conductivity of *p*-poly Si. The leakage current of ATO according to the applied voltage in this DRAM structure was recorded with an HP4140BpA meter at a scanning rate of 0.1 V/s. The leakage current measured was divided by the total number of DRAM capacitor cell to transform it into the leakage current density: leakage current per one unit DRAM capacitor cell (A/cell). The capacitance of the DRAM capacitor was measured by a HP4194A impedance analyzer with a 100 kHz frequency.

Table 1 Optimized ALD deposition temperature and deposition rates for Al_2O_3 and TiO_2 depending on oxidants

Dielectrics	Metal precursors	Oxidant	Optimized process temperature (°C)	Deposition rate (nm/cycle)
Al_2O_3	TMA	O_3	450	0.07
		H_2O+O_3	325 (250–450)	0.11
TiO_2	TIP	O_3	325	0.03
		H_2O	325	0.10

Results and discussion

Optimized ALD conditions for Al_2O_3 thin film

Trimethylaluminum (TMA, $Al(CH_3)_3$) is a typical and ideal precursor for atomic layer deposition of Al_2O_3 because it has a high vapor pressure at ambient temperature, good thermal stability up to 500 °C, and good reactivity with various oxygen sources [14]. Even if TMA shows good reactivity, conformal and uniform deposition might not be achieved due to the oxidants. In case of using H_2O as an oxidant, the deposition rate of Al_2O_3 (thickness increase per one ALD cycle) was 0.11 nm/cycle on the flat surface of Si(100) wafer. The deposition rate was almost independent of deposition temperature. In case of O_3 oxidant, however, the deposition rate of Al_2O_3 varied from 0.09 to 0.07 nm/cycle depending on the deposition temperature from 250 to 450 °C [15]. In addition to the deposition rate, conformal deposition must be confirmed in OCS, which has a deep trench hole with 1,500 nm depth and 150 nm width. Conformal deposition means that thin film was deposited on the trench hole with the same thickness irrespective of position in the trench hole. We tried to form Al_2O_3 thin film with 30 nm thickness target on the trench hole at given deposition temperatures. Then, we measured and compared the thickness of the Al_2O_3 thin film depending on the position in the trench hole of the OCS by SEM. When deposition conditions were not optimized, thin film thickness at the bottom of the trench hole was thinner than that at the top. As one of the criteria for optimized condition for ALD, conformality was defined as the thickness ratio between bottom and top. Figure 2 showed the change of conformality depending on the deposition temperature and given oxidants. When multi-oxidant, simultaneous or sequential feeding of H_2O and O_3 was used as oxidant, Al_2O_3 thin film was deposited uniformly inside the trench hole in all the deposition temperatures given in this experiment (200–450 °C). In case of O_3 oxidant, conformal deposition was achieved only at

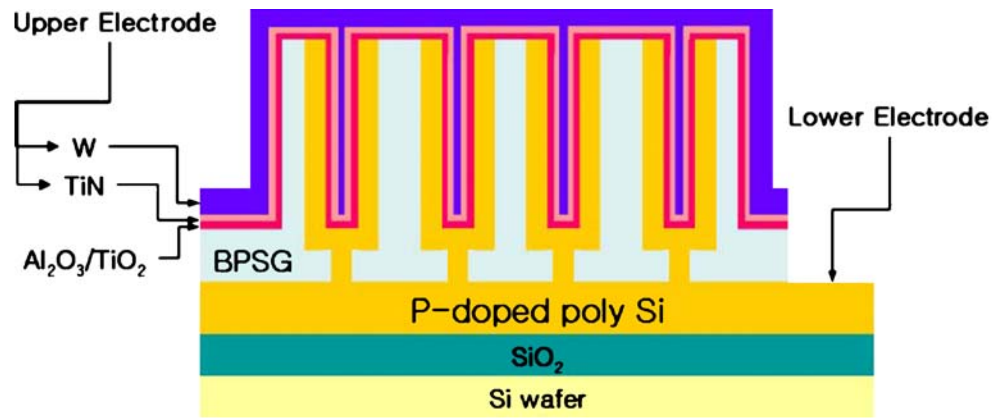


Fig. 1 Schematic cross-sectional view of capacitor structure in DRAM device

450 °C. In the range of temperatures lower than 450 °C, the thickness of the Al_2O_3 film formed by O_3 oxidant at the bottom of the trench hole was thinner than that at the top. Figure 3 compared the leakage current density of the Al_2O_3 thin film by O_3 oxidant with 4 nm target on the OCS with different temperatures. In all range of applied voltage, the Al_2O_3 thin film formed at 250 °C showed higher leakage current density than that at 450 °C. The thickness of Al_2O_3 formed at 250 °C at the top of trench hole in OCS was 4 nm. However, that at the bottom of trench hole might be less than 2.9 nm, assuming the conformality shown in Fig. 2. Thus, the increase of leakage current was attributed to the decrease of Al_2O_3 thickness at the bottom of the trench hole. Conformal deposition of the Al_2O_3 thin film by H_2O or multi-oxidant (H_2O+O_3) was achieved in a wide range of deposition temperatures. However, conformal deposition by O_3 oxidant was accomplished only at higher temperatures (more than 450 °C).

Optimized deposition conditions for TiO_2 thin film by ALD

Figure 4 showed the change of deposition rate for the TiO_2 thin film on Si(100) wafer using titanium isopropoxide (TIP, $Ti(OCH(CH_3)_2)_4$) as a titanium precursor and O_3 as an oxidant. TIP has the highest vapor pressure among titanium alkoxides [16]. So, it has been widely used as a precursor not only in CVD but also in ALD [14, 16]. As the deposition temperature increased from 283 to 360 °C, the deposition rate increased gradually. Above 360 °C, the deposition rate of TiO_2 increased drastically and thickness uniformity within 9 in. wafer also deteriorated abruptly. This is due presumably to the decomposition of TIP. TIP contained oxygen in its molecular structure. Thus, it turns into TiO_2 without an oxidant. In CVD, the stability of the precursor was only needed during the transportation from source reservoir to reactor to protect gas phase reaction. In ALD, however, the source must be stable enough to be adsorbed on the surface of

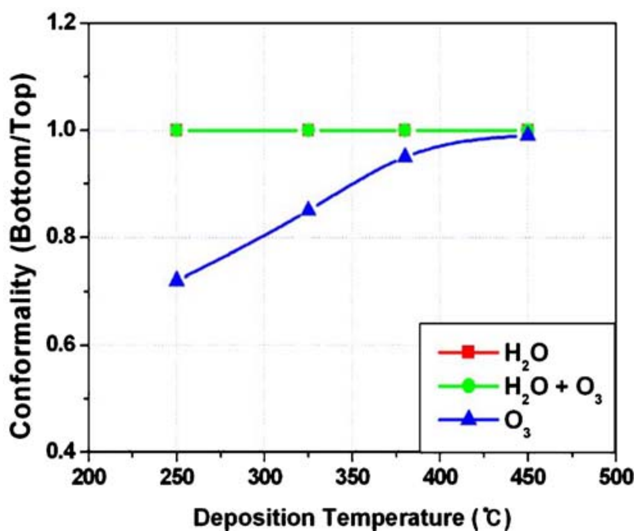


Fig. 2 The change of conformality in deposition of Al_2O_3 depending on the deposition temperature and oxidants

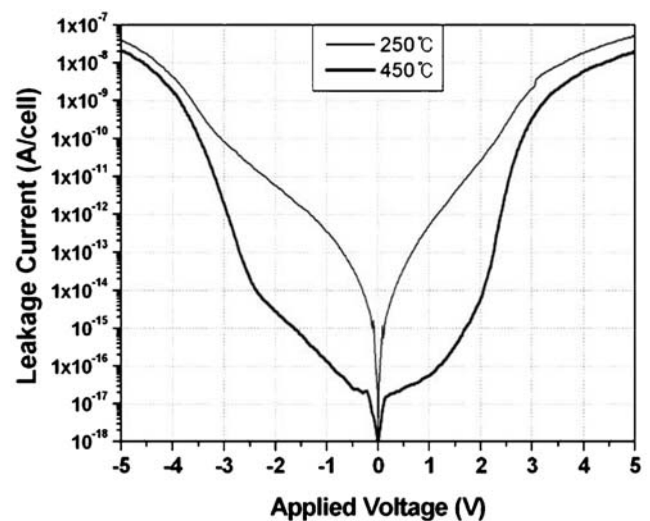


Fig. 3 Leakage current density change of Al_2O_3 by O_3 oxidant on OCS depending on the deposition temperature: 250 °C (*thin line*), 450 °C (*thick line*)

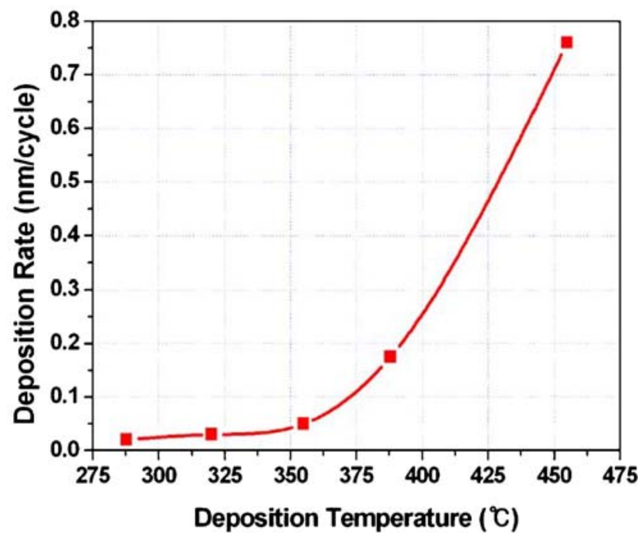


Fig. 4 The change of deposition rate of TiO_2 thin film on Si(100) depending on the deposition temperature

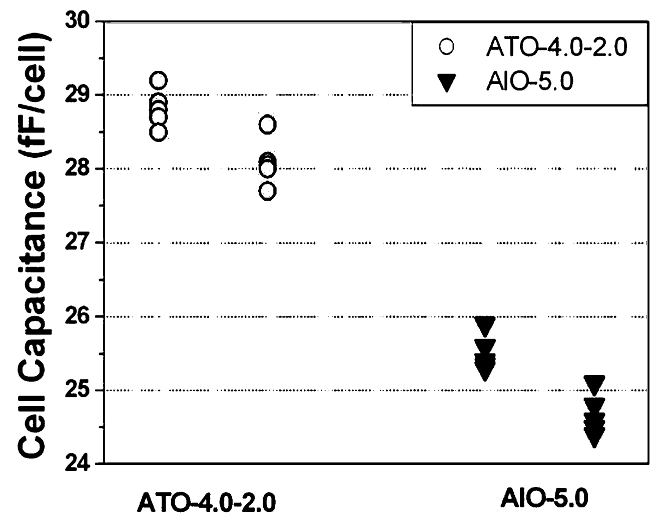


Fig. 6 The change of charge storage capacitance with same DRAM capacitor structure depending on the dielectric thin films

the substrate and must not be decomposed until the oxidant was provided. Self-limiting or self-controlling properties of ALD were lost when self-decomposition of the precursor was dominant in the deposition reaction conditions. Based on these considerations, the CVD mode TiO_2 thin film was achieved when the temperature was more than 360 °C, and that of the ALD mode was accomplished when the deposition temperature was, at least, less than 360 °C [16].

Figure 5 showed the change of conformality and corresponding SEM images of the TiO_2 thin film inside the trench holes of the OCS. The deposition temperature was also the main factor for conformal deposition. At 325 °C, TIP was stable enough to be distributed uniformly on the surface of the trench holes. As the temperature increased up to 450 °C, decomposition of TIP was too fast for TIP to be distributed inside the trench holes. Thus, the TiO_2 film was deposited on the upper part of the trench hole. These results showed that optimized deposition condition of TiO_2 for ALD was achieved when the deposition temperature was less than 360 °C. Considering conformal deposition and deposition rate, deposition temperature should be 325 °C. The optimized ALD conditions for Al_2O_3 and TiO_2 thin film was also summarized in Table 1.

Enhancement of electrical properties by bilayer formation

Based on the optimized deposition conditions mentioned above, Al_2O_3–TiO_2 bilayer (ATO) dielectric thin film was

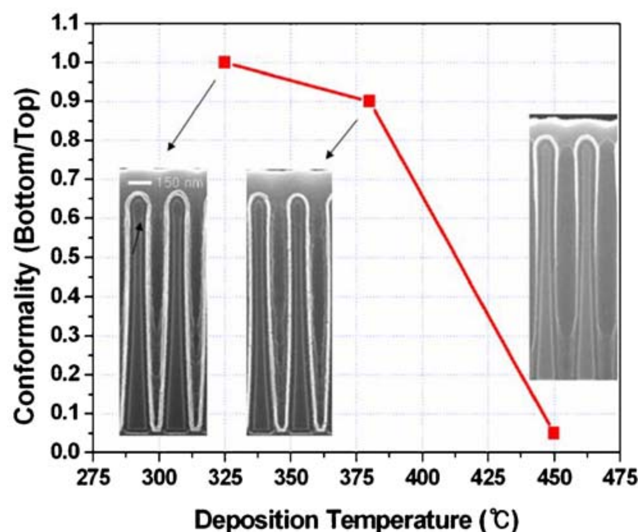


Fig. 5 The change of conformality for TiO_2 in deep trench hole and corresponding vertical SEM images: *thin white layer* in the SEM image was TiO_2 thin film

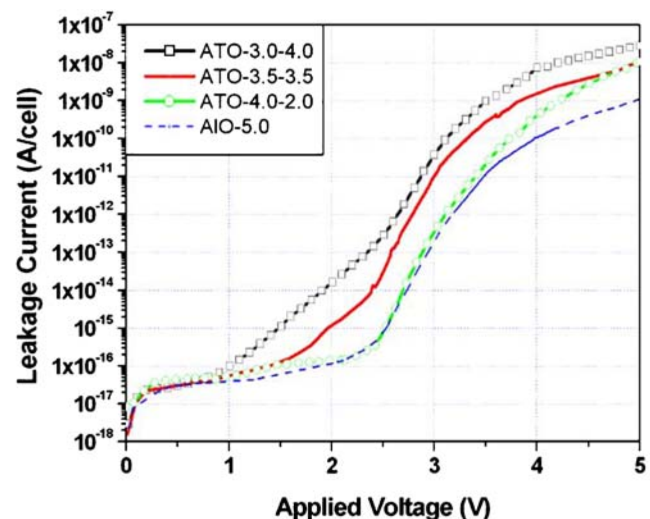


Fig. 7 The change of leakage current depending on the composition of dielectric thin films ATO-3.0-4.0, ATO-3.5-3.5, ATO-4.0-2.0, and AlO-5.0. The upper electrode was TiN/W

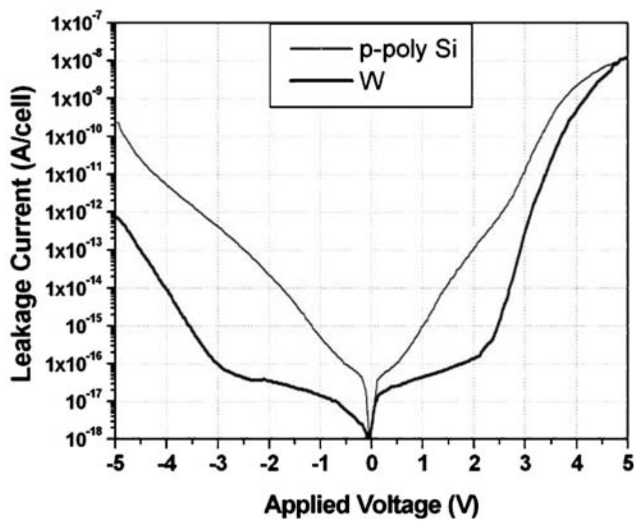


Fig. 8 Comparison of leakage current density of ATO-4.0-2.0 depending on the upper electrode materials: TiN/*p*-poly Si (*thin line*), TiN/W (*thick line*)

deposited on the OCS of *p*-poly Si with trench hole of 1,500 nm depth and 150 nm width. This geometry and deposition orders, as shown in Fig. 1, were intended for the practical application for the DRAM device. Thus, electrical properties measured in this structure must meet the values generally required in the DRAM device. For example, charge storage capacitance of one cell must be larger than 25 fF/cell and leakage current density must be less than 1 fA/cell at the applied voltage of 1.5 V for the stable data storage and operation in the DRAM device. As shown in Fig. 6, cell capacitance of Al_2O_3 with 4.0 nm and TiO_2 with 2.0 nm (ATO-4.0-2.0, 28.5 fF/cell) was 15% higher than that of Al_2O_3 with 5.0 nm thickness (AlO-5.0, 25.0 fF/cell). Total thickness of ATO increased to 6 nm, compared with 5 nm thickness Al_2O_3. However, thickness decrease of low-*k* (~9) Al_2O_3 from 5 to 4 nm finally decreased the effective thickness of the dielectric thin film and resulted in the enhancement of the charge storage capacitance. Figure 7 showed the leakage current of the Al_2O_3 and ATO thin films with various thickness, deposited on the DRAM capacitor structure mentioned above. The leakage current curve for ATO-4.0-2.0 showed almost the same curve compared with that for AlO-5.0. As AlO-5.0 was already proven as a dielectric thin film for the DRAM device [15], ATO-4.0-2.0 also seems to be a reliable dielectric thin film applicable for the DRAM device. In the viewpoint of leakage current, the decrease of 1 nm thickness for Al_2O_3 was compensated by the increase of 2 nm thickness for TiO_2. When the thickness of Al_2O_3 was less than 3.5 nm, however, the addition of TiO_2 with 3~5 nm thickness on Al_2O_3 was not effective for the reduction of leakage current down to that of Al_2O_3 with 5 nm thickness. This result showed that the thickness of Al_2O_3 was the main factor to control leakage current density in ATO dielectric thin film. Summarizing results from Figs. 6 and 7, proper thickness combination of Al_2O_3 and TiO_2 enhanced the charge capacitance without the increase of leakage current.

Change of leakage current depending on the post thermal process

In this section, the effect of post treatment on ATO was investigated for the real DRAM device applications.

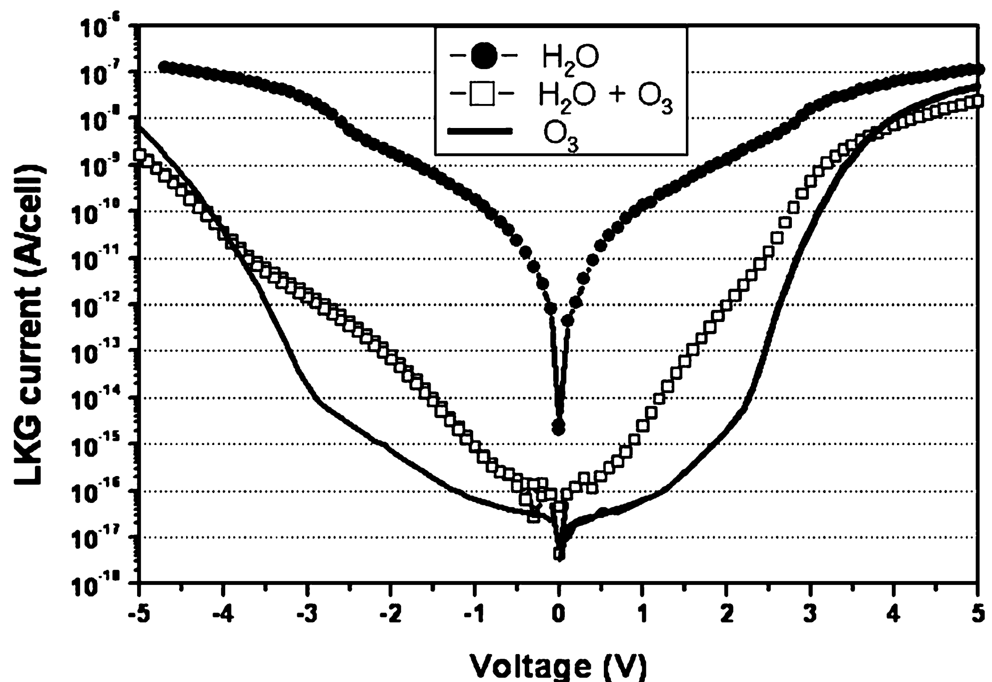


Fig. 9 The change of leakage current density of ATO-4.0-2.0 depending on oxidants: TiN/*p*-poly Si was used as upper electrode and annealed at 600 °C for the increase of conductivity of *p*-poly Si

Figure 8 showed the leakage current change of ATO-4.0-2.0 depending on the deposition materials of the upper electrode. Both of them had almost the same charge capacitance around 28.5 fF/cell. However, the leakage current density of ATO with TiN/*p*-poly Si was much higher than that of ATO with TiN/W. The deposition materials of the upper electrode were closely related with thermal stress imposed on the ATO dielectric thin film. The common first layer of the upper electrode was TiN. W or *p*-poly Si was used as a second layer in the upper electrode. Unlike W, which was deposited by sputter at ambient temperature, *p*-poly Si was deposited at 550 °C. Furthermore, *p*-poly Si was annealed at 650 °C to increase the conductivity. Thus, drastic increase of leakage current for ATO with TiN/*p*-poly Si might come from thermal stress during the second layer formation of the upper electrode. It also indicated that thermal stress should be minimized to prevent leakage current increase.

In case of using TiN/W as upper electrode, three types of oxidants, O_3, H_2O, multi-oxidant (H_2O feeding and subsequent feeding of O_3), did not affect the leakage current density of the ATO thin film. However, when TiN/*p*-poly Si was used as an upper electrode and annealed at 600 °C for the conductivity enhancement of *p*-poly Si, leakage current density of ATO varied depending on the types of the oxidants, as displayed in Fig. 9. ATO formed by O_3 oxidant showed lowest leakage current. ATO by H_2O displayed highest leakage current. It may be attributed to the reaction intermediate during the ATO film formation, particularly, Al_2O_3 thin film. As shown in Eq. (1), well-known reaction mechanism between TMA and H_2O is the exchange reaction between the methyl group in TMA and the –OH group in H_2O [18]. This reaction also produced methane as a by-product. Thus, formation of Al–OH is inevitable during the Al_2O_3 film growth. On the other hand, the proposed reaction mechanism between TMA and O_3 was radical reaction and produced ethane instead of methane. Based on this mechanism, Al–OH did not form during the formation of Al_2O_3 [17, 18].

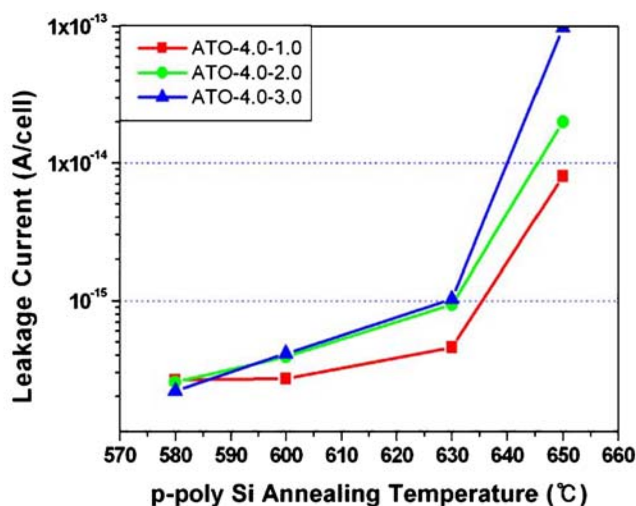
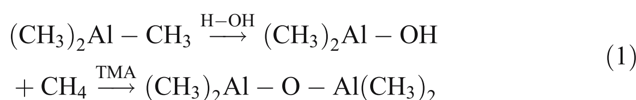
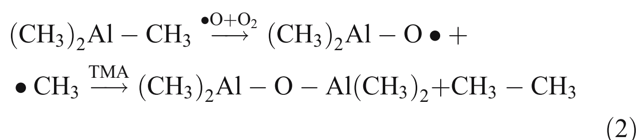


Fig. 10 The change of leakage current density of ATO-4.0-2.0 depending on the annealing temperature for *p*-poly Si

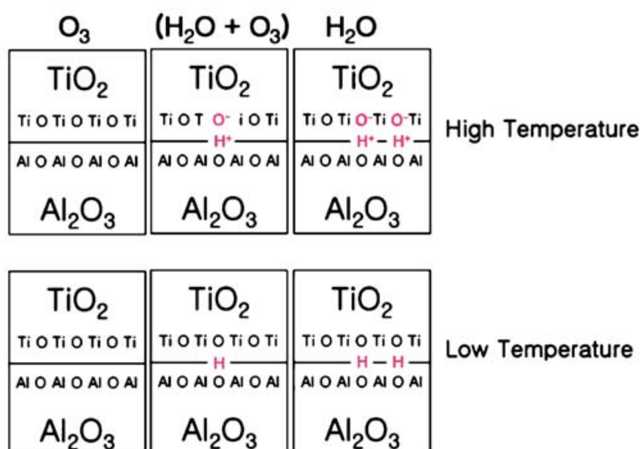


$$(CH_3)_2Al-CH_3 \overset{H-OH}{\longrightarrow} (CH_3)_2Al-OH + CH_4 \overset{TMA}{\longrightarrow} (CH_3)_2Al-O-Al(CH_3)_2 \quad (1)$$



$$(CH_3)_2Al-CH_3 \overset{\bullet O+O_2}{\longrightarrow} (CH_3)_2Al-O\bullet + \bullet CH_3 \overset{TMA}{\longrightarrow} (CH_3)_2Al-O-Al(CH_3)_2+CH_3-CH_3 \quad (2)$$

At higher thermal stress condition, the –OH group that remained in the ATO film might dissociate into $–O^-$ and H^+. These charged species might play as leakage current sources. ATO by combined oxidants (H_2O+O_3) showed lower leakage current than that of ATO by H_2O oxidants. It might be because O_3 that proceeded to H_2O suppressed –OH formation or promote Al–O–Al bonding among the remaining Al–OH groups. Thus, the addition of O_3 might reduce the leakage source in the ATO thin film. The range of conformal deposition condition for Al_2O_3 with H_2O or multi-oxidant (H_2O+O_3) was wider than that with O_3 as shown in Fig. 2. However, only Al_2O_3 formed by O_3 oxidant with a narrow range of process condition was useful when high temperature treatment, such as TiN/*p*-poly Si with 600 °C annealing, was applied on ATO. In addition to the reaction mechanism, previous X-ray photoelectron spectroscopy study by Lee et al. also pointed out that Al_2O_3 deposited by H_2O had interfacial defects between Si and



Scheme 1 Schematic diagram for the change of leakage current depending on oxidants used in the formation of ATO thin film

Al_2O_3 because H_2O has lower reactivity for the Si surface compared with that for O_3 [18]. These types of interfacial defects might also create leakage current sources after higher temperature treatment. Considering previous reports, ALD reaction mechanism and results obtained in this experiment, the leakage current mechanism was summarized and suggested as shown in Scheme 1.

Although, ATO film formed by O_3 showed lower leakage current than those of ATO by other two oxidants, high temperature treatment gave a detrimental effect on ATO in leakage current density. Figure 10 showed the change of leakage current density for ATO formed by O_3 oxidants, depending on the annealing temperature for *p*-poly Si. The leakage current density was measured at 1.2 V. Annealing temperature and TiO_2 thickness raised leakage current density. To minimize leakage current density, annealing temperature must be less than 630 °C to meet the minimum requirement of the DRAM device: 1×10^{-15} A/cell.

In the viewpoint of capacitor dielectric materials, low temperature processes, such as W deposition by sputtering at ambient temperature, were preferred because they did not induce stress on capacitor dielectric thin film. High temperature processes, for example, *p*-poly Si by CVD at 550 °C and subsequent annealing at 650 °C, induced much stress on the ATO thin film, which resulted in the drastic increase of leakage current density. With respect to the fabrication for the DRAM device, however, *p*-poly Si might be a more productive and cost-effective material than W because *p*-poly Si was already applied in the DRAM device and no additional investment for deposition machines were required, depending on the typical conditions for mass production fabrication line. To meet the requirement for effective integration of DRAM devices and enhancement of electrical properties of dielectric thin film simultaneously, deposition conditions and post thermal process must be optimized and balanced based on a series of experimental results described above. In case of using TiN/W as upper electrode, ATO, formed by various types of oxidants, can be used as dielectric thin film in the capacitor with low leakage current density. However, TiN/*p*-poly Si was forced to be used as upper electrode for effective device integration for DRAM, annealing temperature for *p*-poly Si must be less than 600 °C and oxidant for ATO thin film formation must be O_3 to enhance charge storage capacitance without increase of leakage current density.

Conclusions

Conformal and uniform deposition conditions for Al_2O_3 and TiO_2 was set for DRAM capacitor structure. Based on these conditions, ATO-4.0-2.0 increased the charge storage capacitance by 15% without increase of leakage current compared with that of AlO-5.0. When TiN/W was used as an upper electrode, the increase of charge storage capacitance was achieved without leakage current density regardless of oxidants. However, when TiN/*p*-poly Si with additional annealing was used as an upper electrode, the leakage current density of ATO increased drastically. ATO by O_3 had relatively lower leakage current density than that of ATO by H_2O or combined oxidant (H_2O+O_3). ATO deposition conditions and post thermal treatment were selected and optimized depending on the requirement of DRAM devices.

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